Research Highlight

Microsecond Resolution X-ray Imaging Tests of a Pixel Array Detector

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Recently introduced electronic area X-ray detectors (such as CCD based detectors) are having an enormous impact within the experimental x-ray community. The efficiency and ease of data collection has been improved considerably. They are also making practical the implementation of powerful new methodologies in data collection such as fine rotation slicing of crystallography data or multi-wavelength anomalous diffraction (MAD) phasing.

Development of new detector technologies promises to extend the capabilities of area detectors even further. One such effort is taking place within Prof. Sol Gruner's detector group in the Laboratory of Solid State and Atomic Physics (LASSP) at Cornell University. Under development is a detector, based entirely on silicon, with imaging rates of up to one million frames per second (Figure 1). Known as a Pixel Array Detector (PAD), the detector is configured such that each pixel contains sufficient circuitry to perform the high-speed imaging. This CMOS chip is designed and fabricated using industry standard integrated circuit design tools, yielding a set of instructions which is sent to a silicon chip fabrication service. This paper is a description of high-speed imaging tests made with a 92 by 100 pixel prototype detector at CHESS during December 1998. More in-depth details can be found in [1].

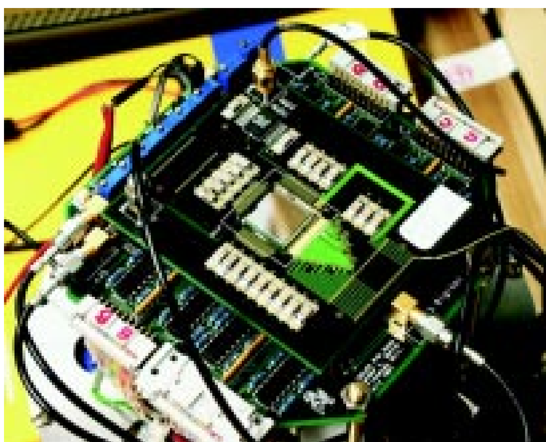

Figure 1: Pixel Array Detector (PAD). The 100 by 92 pixel prototype detector and associated electronics is shown in the uncovered cryostat. The detector chip is the mirror-like square in the center of the printed circuit board. The detector consists of an array of 150 x 150 micron^2 diodes bonded to an underlying CMOS electronic layer with in-pixel integration and storage capabilities.

The detector

This detector is actually a sandwich of two silicon wafers (Figure 2). The first, the X-ray sensitive layer, is a special high resistivity silicon wafer into which an array of 150 by 150 micron^2 diodes is fabricated. X-rays stopping in silicon produce a large signal (ca. 2700 electron/hole pairs per 10 keV X-ray) which can be collected quickly (nanoseconds). The high resistivity wafer permits the X-ray generated signal to be collected from a depletion layer of greater thickness than is possible in a typical silicon wafer (> 300 micron thickness vs. 10 micron), greatly enhancing the detection efficiency for X-rays (charge generated outside of the depletion layer quickly recombines and is lost). A custom fabrication service which specializes in low dark current devices (10 fA/pixel at –20 C) was contracted to produce these wafers.

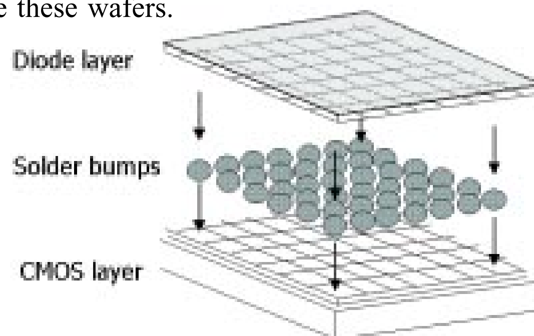

Figure2: Schematic of detector assembly. The PAD is comprised of two silicon wafers electrically connected using an array of solder bumps, one solder bump for each pixel. The top layer is a high resistivity wafer into which an array of X-ray detection diodes is fabricated. Charge generated by the conversion of X-rays in this layer is passed through the solder bumps into the CMOS electronics layer with integration and storage electronics built into each pixel.

The second layer is a standard CMOS electronic chip, which incorporates into each pixel integration, frame storage, and readout electronics. Each pixel has a direct connection with a corresponding diode in the detection layer through an array of solder bumps. The low-temperature solder is patterned with lithographic techniques onto the CMOS chip. The diode layer, with a corresponding array of lithographically formed metallized pads, is brought into alignment with the CMOS layer, where upon the two are joined using modest pressure and temperature.

Charge generated within the detection layer is collected at the input node of the pixel where an amplifier analog integrates the signal onto the main 2 pF storage capacitor (Figure 3). Each pixel also has an array of eight secondary capacitors, which serve as on-chip storage for eight frames. For each frame, one of the eight secondary storage

capacitors is connected to the integration capacitor, sampling its integrated voltage. After it is isolated via CMOS switches, the main capacitor is reset, the next capacitor in the sequence is connected, and the next integration is begun. The dead time between frames can be as low as 0.8 µs. A reconfigurable state machine (off-chip) is used to sequence the necessary resets, delays and switch closings.

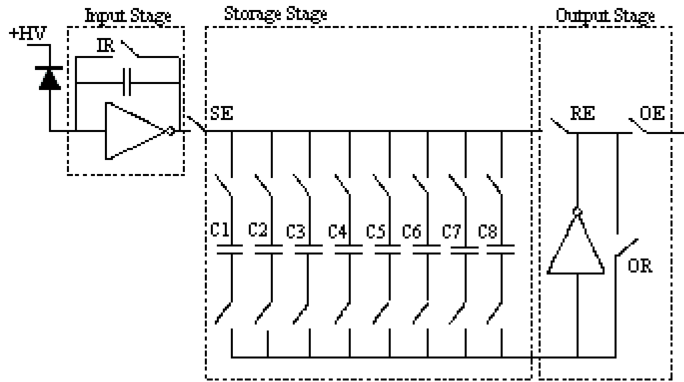

Figure 3: Pixel circuitry schematic. Shown is the electronics integrated within the footprint of each pixel. Charge produced by X-rays in the detection diode layer is integrated onto the capacitor in the input stage. One of eight frame storage capacitors (C1 – C8) is selected using CMOS switches to store the integrated voltage level for each frame. Rapid imaging of up to eight frames is accomplished through the proper sequencing of these capacitors in concert with integration reset (IR). Frame readout is accomplished by connecting the storage capacitors in sequence with the output amplifier. SE, store enable; RE, read enable; OE, output enable; OR, output reset; IR, input reset.

Once the detector has recorded the eight frames, the secondary storage capacitors are sequentially connected to an output amplifier incorporated into each pixel. Pixels are multiplexed to an additional amplifier at the edge of the CMOS chip, which buffers the signal to the A/D converter. Although the design could readily incorporate a highly parallel digitization, only a single A/D channel was used in this prototype device.

The CMOS layer in this detector was fabricated using a process with 1.2 micron minimum feature size. As has been done for the smaller scale test structures leading up to the current device, the fabrication was coordinated through the MOSIS service which allows a large community open access to silicon foundry services by pooling small projects together into a single fabrication project. This is the only way such small scale testing can be made economically feasible. The current detector utilized the maximum area available, making this particular fabrication run (yielding 100 pieces) dedicated to our project.

The Tests

Testing the fast frame imaging capabilities of this prototype required the intense X-ray flux available at a synchrotron. Several tests were made at the CHESS D-1 bending magnet beamline. The first test used a 1% bandwidth multilayer monochromator to provide a beam suitable for small-area, time-resolved radiography. In this case, the radiological "subjects" were the teeth of a rapidly spinning, circular-saw blade (180 mm diameter, fine-toothed plywood blade). The 8.9 keV X-ray beam illuminated an area of 1.7 by 12 mm^2 (12 by 80 pixels) with a flux of > 10^{10} X-rays/pixel/s. Attenuation was used to vary the incident flux on the detector. The circular saw was mounted in front of the detector such that three of the 2.5 mm high teeth would be shadowed within the beam area. The saw was plugged into a variable transformer outside the hutch which controlled the rotation speed. Shown in Figure 4 are the first three images of a set taken with a 5 µs integration time and a 1 µs interframe delay. Flux in these exposures was 2 x10^9 X-rays/pixel/s. The three dark triangular regions pointing up are the saw teeth. Even at the maximum rotation speed of 5000 RPM, each saw tooth travels just 0.3 pixel/µs.

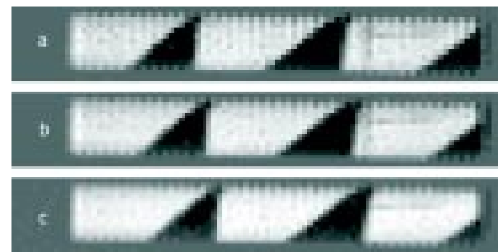

Figure 4: Radiography of a moving saw blade. Shown are portions of three successive frames with 5 microseconds integration time and 1 microsecond interframe delay. The X-ray beam illuminated an area of roughly 12 x 80 pixels on the detector. The saw teeth are the dark triangular regions pointing upward in these images. The rotation rate of 5000 RPM corresponds to a linear speed of 48 m/s for the saw teeth. No intensity uniformity correction has been applied to these images.

The detector was also evaluated in a time-resolved transmission Laue diffraction experiment. Here the beamline was configured to allow the white beam onto a rapidly rotating (2500 RPM) disk of 1.5 mm thick polycrystalline aluminum sheet metal (type 3003). The beam was set to 1 x 1 mm^2 and the sample to detector distance was 30 mm. Shown in Figure 5 is a set of 8 images with 100 µs integration time and 25 µs interframe delay. Although the beam is passing through many crystallites in each frame, the crystallites are generally oriented along the same axis. The change in pattern observed is the change in the orientation axis as the sample is rotated.

This prototype device was by no means perfect, nor did we expect it to be. The available beam was easily able to deliver enough X-rays to fill the pixel well (17000 X-rays) within a microsecond. When taken together with the pulsed nature of the synchrotron, the instantaneous currents from the diodes were a significant fraction of the maximum current the input amplifier could drive. Not surprisingly (in hindsight anyway), transient shifts in the pixel bias were observed at these highest levels of illumination. Interestingly, the minimum frame time of the device allows the longest time structure of the synchrotron to be observed.

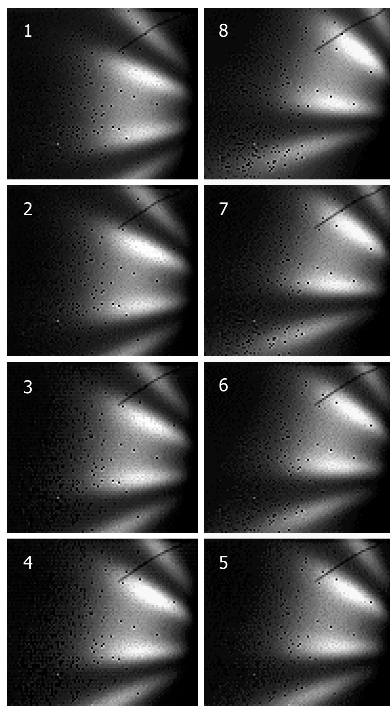

Figure 5: Time resolved Laue diffraction from polycrystalline aluminum sample. A 1.5 mm thick disk of type 3003 aluminum was placed in a 1 x 1 mm^2 white beam. The 180 mm diameter disk was rotating at 2500 RPM with the beam sampling a volume 10 mm from the edge of the disk. Diffraction features are the superposition from many oriented grains within the sample. The 8 images shown were obtained as the disk rotated through 15 degrees. Integration time was 100 µs per frame with 25 µs interframe time between integration periods. The time sequence is labeled 1 to 8 on each frame. Frame 8 is placed next to frame 1 to highlight the change in diffraction seen. The shadow of a small, thin wire used to bias the diodes appears in each image in the upper right region.

Another interest was the short and long term effects of radiation damage. Although shielded by the overlaying detection diodes, the CMOS layer still receives a significant x-ray dose when used in conjunction with the intense beams needed for high speed imaging (10 krad/s in the tests above). It is thought that the primary mechanism for damage is through a buildup of immobile charge in the gate oxides as they become exposed to high doses of X-rays (ca. 100 krad). This shifts the potentials of the transistor controlling gates, changing their properties, and eventually rendering them inoperable. Further shielding of the CMOS chip might be possible through clever placement of components under suitably large solder bumps. The most promising improvement to radiation tolerance seems to be coming as a byproduct of the continued miniaturization (to increase density) of the standard CMOS process. As the feature size of transistors shrink, so do the oxide dimensions. In fabrication processes with feature sizes of 0.25 micron and below, the oxide has become sufficiently thin so that otherwise immobile charge has a significant probability to quantum-mechanically tunnel out of the oxide layer. Circuits fabricated with such processes have been shown to be orders of magnitude more radiation tolerant.

Future Developments

This detector architecture facilitates application specific customizations of the inner workings of each pixel. One can develop new in-pixel structures independently in small-scale, inexpensive test fabrications, without the need to re-engineer the detective layer, the solder bump connections, or many other common issues regarding the architecture. Indeed, there are other groups throughout the world working on detectors similar in concept with vastly different in-pixel architectures [2]. In contrast to the effort described here, many of these are using photon counting circuitry within each pixel. One might envision on-board time or space correlators or high speed differencing circuitry as well.

There are plans to fabricate test structures using the smaller feature size processes. Not only do we hope to mitigate radiation damage, the smaller features allow more sophisticated circuitry to be contained within the footprint of each pixel. We hope to increase the dynamic range (currently 14 bits/frame) as well as improve noise immunity. One of the major engineering tasks remaining is scaling the size of the detector to dimensions useful to a wider class of diffraction problems. Increasing dimensions to 1000 x 1000 pixels or greater will probably require tiling smaller sub-units together.

References

[1] Rossi, G., Renzi, M., Eikenberry, E. F., Tate, M. W., Bilderback, D., Fontes, E., Wixted, R., Barna, S. and Gruner, S. M. Tests of a Prototype Pixel Array Detector for Microsecond Time-Resolved X-ray Diffraction
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[2] Datte, P., Birkbeck, A., Beuville, E., Endres, N., Drouillole, F.,.Luo, L, Millaud, J. and Xuong, N-H. *Nucl. Instrum. Meth.* A **421**, 576-550 (1999)